

Practical Application of the Verification Methodology Manual Using SystemVerilog

Overview

Practical Application of the Verification Methodology Manual Using SystemVerilog is a 1-day comprehensive training course on the practical definition of a SystemVerilog transaction-based testbench compliant to the “*Verification Methodology Manual for SystemVerilog*” (VMM) by Janick Bergeron, et. al. A FIFO design is used to illustrate using the VMM methodology for the creation of a comprehensive constrained-random verification environment. This includes the generation of transactions and the consumption of transactions via transactors, the definition of the verification environment, the monitor, the scoreboard, the factory and callback methods, directed tests, custom generator. Labs reinforce these VMM concepts. Students receive a comprehensive training guide that will serve as an invaluable aid in applying the concepts in the book “*Verification Methodology Manual for SystemVerilog*”.

Practical Application of the Verification Methodology Manual Using SystemVerilog is a VHDL/Cohen training course developed and presented by Ben Cohen. This course is offered through Sutherland HDL, but is not a Sutherland HDL training course. Ben Cohen is a well known author of VHDL, Verilog and SystemVerilog books, and an experienced design and verification engineer.

Course Objectives

At the conclusion of this workshop, engineers will understand how to use SystemVerilog to apply the complex verification methodology recommended in the book “*Verification Methodology Manual for SystemVerilog*” by Bergeron, Cerny, Hunter, and Nightingale.

Intended Audience

This workshop is for verification engineers who are already familiar with the SystemVerilog testbench constructs. The course presupposes a working knowledge of Verilog and the SystemVerilog testbench enhancements to Verilog. Engineers who are not familiar with SystemVerilog should first take Sutherland HDL's “*SystemVerilog Testbench for Verification Engineers*” workshop.

Prerequisites (essential)

Knowledge of the SystemVerilog testbench constructs is mandatory! Without this prerequisite knowledge, students cannot fully benefit from this workshop. Familiarity with SystemVerilog Assertions is beneficial.

Software Tools Used

The Cadence *Incisive*[™], Synopsys *VCS*[™] or the Mentor Graphics *Questa*[™] simulator will be used for labs.

Workshop Locations

This workshop can be presented on-site, at your facilities. We also offer several open-enrollment workshops throughout the year. For more information, please refer to our web page, www.sutherland-hdl.com, or call us at +1-503-692-0898.

Syllabus — Practical Application of the Verification Methodology Manual Using SystemVerilog

Day One

Section 1: VMM Transactions and Channels

- Why a verification framework
- Testbench architecture
- Elements of a testbench in framework
- Transactions
- Channels
- Environment
- Lab 1

Section 2: Transaction Generator and Transactor

- Elements of a testbench in framework
- Transaction generator
- Transactor
- Lab 2

Section 3: Building the Environment

- Verification environment
- Programs
- Testbenches
- Simulation
- Lab 3

Section 4: Using the Factory Method

- Factory definition
- Factory applications
- Factory method
- Allocation
- Lab 4

Section 5: Callback

- Callback definition
- Callback applications
- Callback method
- Lab 5

Section 6: Advanced Framework

- Custom generator
- Directed tests
- Monitors and Scoreboards
- Ending the simulation
- Lab 6