

Advanced SystemVerilog Open Verification Methodology (OVM)

Overview

Advanced SystemVerilog Open Verification Methodology is a 3-day comprehensive training course on how to create complex high-level verification environments using SystemVerilog and the OVM class libraries.

The *Advanced SystemVerilog Open Verification Methodology* course is offered through Sutherland HDL, but is developed by—and is presented by—Willamette HDL. Sutherland HDL has a partnership agreement to arrange this workshop in behalf of Willamette HDL as an adjunct to Sutherland HDL's SystemVerilog verification workshops.

Course Objectives

At the conclusion of this workshop, engineers will understand how to use SystemVerilog to apply the complex verification methodology recommended in the book “*OVM Open Verification Methodology Cookbook*” by Mark Glasser.

Intended Audience

This workshop is for verification engineers who are already familiar with the SystemVerilog testbench constructs. The course presupposes a working knowledge of Verilog and the SystemVerilog testbench enhancements to Verilog. Engineers who are not familiar with SystemVerilog should first take Sutherland HDL's “*SystemVerilog Testbench for Verilog Verification Engineers*” or “*SystemVerilog Testbench for non-Verilog Verification Engineers*” workshop.

Prerequisites (essential)

Completion of Sutherland HDL's SystemVerilog Testbench workshop, or equivalent knowledge, is mandatory before taking this advanced workshop! Without this prerequisite knowledge, students cannot fully benefit from this workshop.

Course contents

A full description of this workshop can be found at: www.whdl.com.

Workshop Locations

This workshop is only available as on-site training held at your facilities.