

Comprehensive VHDL for Synthesis and Verification

Overview

Comprehensive VHDL for Synthesis and Verification is a 4-day workshop covering the aspects of the IEEE 1076 VHDL standard and IEEE 1164 Standard Logic standard that is useful for synthesis modeling and test benches. The design style focus is on using VHDL for top-down design with synthesis and simulation. Special attention is given to working with subtleties of the language, such as how to work with different types, operator overloading and usage of pre built packages. The importance of coding style, design verification and documentation are also emphasized. A student guide, reference sheets and the book *“The Designer's Guide to VHDL”* by Peter J. Ashenden are included.

The primary focus of the workshop is two fold. First is on writing synthesizable VHDL models for simulation. Second is on writing the simulation test bench for each lab. Several simulation labs reinforce the principles presented. Sixty five percent of the class time is devoted to hands-on experience, as engineers model and simulate a number of small hardware circuits. At the conclusion of this workshop, engineers will have the modeling and verification skills to immediately be productive in writing, simulating and synthesizing VHDL models of hardware designs.

Presented By

Don Mills. Mr. Mills is an independent consultant with extensive experience in the top-down design and synthesis of ASICs, using CMOS and ECL technologies.

Software Tools Used

Students will be using VHDL simulation tools during class labs. On-site training will cover what ever simulator is provided in the training lab. Workshops using Sutherland HDL's portable lab equipment use the Mentor Graphics *ModelSim* simulator.

Intended Audience

VHDL for Synthesis and Verification workshop is for digital engineers who will be designing ASICs, FPGAs or systems with VHDL. The workshop enables students to immediately be productive with the VHDL language and VHDL software tools. Both new VHDL users, as well as those who are familiar with VHDL and desire a more in-depth knowledge of the intricacies of VHDL, will benefit from this course.

Prerequisites (essential)

Knowledge of digital design engineering is required. Without this background, students cannot fully benefit from this course. Labs include writing VHDL models of digital circuits such as shift registers, arithmetic logic units, and FSMs.

Comments From Students

“The best part of the course was state machines, type conversions, composite data types, test benches, and large design techniques.”

“Lecture half day and lab half day is perfect.”

“I liked the one on one personal help with labs and answering questions.”

Workshop Locations

This workshop can be presented on-site, at your facilities. We also offer several open-enrollment workshops throughout the year. For more information, please refer to our web page, www.sutherland-hdl.com, or call us at **1-866-HDL-XPRTS** (1-866-435-9778). From outside the US, please call +1-503-692-0898.

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Syllabus — Comprehensive VHDL for Synthesis and Verification

Day One

Introduction to VHDL

- Concepts of top-down design
- Basic building blocks of VHDL
- Entity declarations
- Architecture bodies
- Formatting notes
- Comments
- Identifiers
- Numbers
- Characters and strings
- Bit strings

Scalar Data Types and Operations

- VHDL objects
- Declarations
- Constants and variables
- Types and type declarations
- Operators
- Operator overloading
- Std_Logic 1164 type
- Sub types
- Type conversion

Processes, Sequential Statements, and Test Benches

- Process basics
- Sequential statements - IF, CASE, LOOP
- Test bench introduction
- Test bench configuration
- Labs: Combinational logic designs

Day Two

Composite Data Types and Operations

- Composite types
- Arrays
- Array aggregates
- Array attributes
- Bit vectors and Std_LOGIC arrays
- Array operations and referencing

Putting all the Pieces Together

- Entities
- Architectures
- Processes
- Signal declarations, assignments, and attributes
- Introduction to FF models
- Synchronous and asynchronous FFs
- More on test benches
- Labs: Combinational and sequential logic designs

Day Three

Timing Delays in Processes

- Wait statements
- Delta delays
- Transport and inertial delays

Concurrent Signal Assignment Statements

- Direct assignments
- Conditional assignment
- Selected assignment

Subprograms

- Procedures
- Procedure declaration
- Procedure body
- Procedure parameters
- Functions
- Function declaration and body
- Pure and impure functions
- Overloaded functions
- Labs: More sequential logic designs

State Machines

- Coding styles for state machines
- Labs: State machine designs

Day Four

VHDL Miscellaneous Topics

- Packages and package bodies
- Library and use clauses
- Pre-built packages
- Resolved data types and signals
- Components
- Configurations

Generics and Generate Statements

- Generic constants declaration
- Generic constant redefinition
- For generate statement
- IF generate statement
- Labs: Generics and generates

ASIC Design Methods & Introductions to Synthesis

- Latch coding styles
- How to avoid latches
- Clock zones and synchronous design
- Synthesis constraints
- Synthesis reports
- Synthesis guidelines