Verilog Is Not Called Verilog Anymore! The Merging of the Verilog and SystemVerilog IEEE Standards

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***Abstract*—Over the past 18 months the IEEE has been working to merge the Verilog (IEEE 1364) and SystemVerilog (IEEE 1800) standards into a single standard. The "Verilog" name disappears. The merged standard refers to the entire language as "SystemVerilog". This paper provides a description of what the proposed merged standard will look like, and what new features are being added in the next version of SystemVerilog.**

I. The Evolution of Verilog

The Verilog Hardware Description Language (Verilog HDL) was first created in 1984 and 1985 as a proprietary language for use with the Gateway Design Automation "Verilog" digital simulator (later renamed to "Verilog-XL"; Gateway merged with Cadence Design Systems in 1989). A lot has happened in the world of digital design since 1985! When Verilog was first created, ASIC based chips were in their infancy. The average process geometry was 5 microns, and a chip with 10,000 gates was considered a very large design. As Moore's Law predicted, integrated circuits have doubled in complexity and number of transistors every 18 to 24 months. Today, multi-million gate chips are designed using 45 nanometer and smaller geometries.

The Verilog HDL did not sit idle during this rapid evolution of digital design. It, too, evolved. Every few years a new generation of the Verilog language has been released, with new language features that enabled hardware engineers to keep pace with advances in digital design. Around 1988 and 1989, Gateway Design Automation added features such as specify blocks and nonblocking assignments to enable more accurate RTL and gate-level simulations. In 1990, Verilog was made an open language and Open Verilog International (OVI) took control of the language, releasing OVI Verilog 1.0[1]. In 1992, OVI released OVI Verilog 2.0[2] with several new extensions to Verilog, and turned control over the language to the IEEE. The IEEE released the Verilog-1995 (IEEE Std 1364-1995[3]) standard. In 2000, the IEEE completed adding major enhancements and extensions to Verilog, which became Verilog-2001 (IEEE Std 1364-2001[4]).

Even with these frequent and substantial evolutions of the Verilog standard, it was difficult to keep pace with Moore's Law. To accelerate the evolution of Verilog language evolution, Accellera, a consortium of digital design companies and Electronic Design Automation (EDA) tool vendors, put together a special committee to more quickly define the next generation of extensions design engineers needed for HDL-based design. In 2003, just two short years later, Accellera released the "SystemVerilog 3.0"[6] reference manual. This manual specified several dozens of important extensions to the Verilog-2001 HDL. Most of these extensions targeted modeling, simulating, and synthesizing digital designs.

SystemVerilog 3.0 was not a complete, stand-alone language standard. It was a set of extensions to the IEEE Verilog language. This meant that, to use SystemVerilog, two reference manuals were needed: the Verilog base language and the SystemVerilog extensions. The goal of Accellera when SystemVerilog 3.0 was released was that eventually these two manuals would be merged together into one document.

Before merging the Verilog and SystemVerilog manuals together, however, Accellera wanted to specify more essential extensions. One year later, in 2004, Accellera released SystemVerilog 3.1[7], which added a substantial set of verification extensions to the Verilog-2001 language. Once again, the SystemVerilog manual only defined the language extensions. Users of Verilog and implementors of Verilog software tools needed to keep two manuals open, in order to have access to both the base language and all the new extensions.

Accellera continued refining the many extensions to Verilog during early 2004, and in June 2004 released SystemVerilog 3.1a[8]. Accellera then donated this version of

the Verilog extensions to the IEEE for full standardization. In order to expedite the standardization process, the IEEE decided to postpone merging the SystemVerilog extensions into the Verilog standard. Instead, in 2005, the IEEE released a pair of Verilog-based standards, Verilog-2005 (IEEE Std 1364-2005[5]) and SystemVerilog-2005 (IEEE Std 1800-2005[9]).

As a point of interest, the IEEE Std 1364-2005 Verilog standard (the base language) is 592 pages. The IEEE Std 1800-2005 SystemVerilog standard (the extensions to Verilog) is 664 pages.

II. The Demise of the Verilog Name

While having the extensions to Verilog specified as a separate standard achieved the goal of quickly standardizing and ratifying these extensions, it still meant that Verilog users and tool implementors needed to use two complex reference manuals at the same time, in order to work with the latest extensions to the language. This can be advantageous. Having the extensions to Verilog documented in a separate manual makes it easier for those already familiar with Verilog to find information on just the latest extensions. There is also a disadvantage. Having the full language split into two manuals resulted in redundancy, missing specifications, and occasionally conflicts between the documents.

The IEEE did not pause after releasing the 2005 standards. Discussion began immediately regarding merging the two manuals together. There was considerable debate within the IEEE as to whether this work should be done. Some Verilog and SystemVerilog committee members liked the advantage of documenting all extensions separately from the base language. Others worried that the merge process would introduce errors in the standard that might be time-consuming to correct—time that could be better spent defining additional enhancements to Verilog. Another concern was the cost of merging the documents. While most work within the Verilog and SystemVerilog standards committee is volunteer labor, the editor is a paid contractor. The merge process would involve hundreds of hours of editing, and therefore be expensive.

The IEEE ultimately decided that the advantages of merging the Verilog and SystemVerilog manuals together outweighed the disadvantages. Work began in early 2007, and a draft of the merged document was published within 60 days. Extensive reviews and clarifications were made, and by the end of 2007 a merged document was nearly completed.

No more Verilog! When the IEEE made the decision to merge the Verilog and SystemVerilog manuals, the IEEE 1364 Verilog working group was shut down, and all work was moved into the IEEE 1800 SystemVerilog working group. This means that the name of the merged standard is "*SystemVerilog*". Within the standard, the name "*Verilog*" is no longer used, except to refer to earlier versions of the language.

The demise of the name *Verilog* does not mean the end of Verilog-based design; it simply marks the end of using one name for the language and the beginning of using a new name.

III. Summary of Verilog Generations

The evolution of the Verilog HDL can be divided into five major generations. Note that these generations are of the author's own devising.

- ***First generation:*** Verilog-1985 through Verilog-1995.
  First specified as a proprietary language in 1983, released to the public in 1990, and standardized by the IEEE in 1995 as IEEE Std 1364-1995[3]; a number of incremental enhancements were added during this 12 year period.
- ***Second generation:*** Verilog-2001.
  Officially IEEE Std 1364-2001[4]; contained a significant number of extensions to Verilog-1995. (See [11] for details on the specific enhancements added in Verilog-2001).
- ***Third generation:*** Verilog-2001/SystemVerilog 3.0.
  All extensions were specified in the separate SystemVerilog reference manual and did not have IEEE ratification. The extensions focused on new hardware modeling capabilities.
- ***Fourth generation:*** Verilog-2005/SystemVerilog-2005.
  The IEEE Std 1364-2005[5] Verilog reference manual had relatively few major extensions over Verilog-2001, such as the **`uwire`** type, **`$clog2`** and other math system functions, encryption, a **`'pragma`** directive, and a **`'begin_keywords`** compatibility directive. IEEE Std 1800-2005[9] SystemVerilog added more than 100 major extensions to the design and verification capabilities of Verilog. See [12] and [13] for details on the substantial enhancements contained in SystemVerilog.
- ***Fifth generation:*** SystemVerilog-2008.
  Merges the IEEE 1364-2005 Verilog reference manual and the IEEE 1800-2005 reference manual into a single document, proposed IEEE P1800-2008[10]. Officially, there is no longer a "Verilog" language; it is now referred to as "SystemVerilog". This generation also includes a large number of minor and major enhancements beyond what was in SystemVerilog-2005, along with corner-case clarifications. Many of these enhancements are listed in the following section.

IV. New Extensions Planned for SystemVerilog-2008

In parallel with the merge process, the IEEE SystemVerilog standards committee worked on defining several new extensions to Verilog. Work on these extensions was not quite complete at the end of 2007, but is expected to be finished in early 2008, shortly after this conference. Once the enhancements are defined, the process of IEEE balloting and ratification will begin, which can take several months. The SystemVerilog working group has a goal of completing the entire process before the end of 2008.

The following list highlights 46 enhancements planned for the proposed next generation of SystemVerilog. Note that:

a) This list is not all inclusive. In addition to the enhancements listed, there are many other changes and clarifications in the proposed SystemVerilog-2008 standard.

b) This list is subject to change. At the time this paper was written, the proposed P1800-2008 standard was still being defined, and had not been balloted and ratified.

c) While the IEEE SystemVerilog working group's goal is for a SystemVerilog-2008 standard, the ballot process could take longer than expected, slipping the date to a SystemVerilog-2009 standard.

Enhancements already approved for inclusion:

At the time this paper was presented at DVCon 2008 (21 February 2008), the proposals for 35 of the 46 new features planned for the proposed SystemVerilog-2008 standard had been fully completed and had been approved by the IEEE P1800 SystemVerilog Working Group.

1. *Defining parameter values using configurations.*

   In Verilog-2005, parameter values can only be redefined in-line with module instances, or hierarchically using a defparam statement. This enhancement allows parameter values to also be redefined from within configuration blocks. *(Mantis[1] 2037)*

2. *Default parameter assignment made optional.*

   The proposed SystemVerilog-2008 standard allows parameters to be declared without assigning a value to the parameter. The value for these parameters must be defined when the design block containing the parameter is instantiated. *(Mantis 907)*

3. *Package import in design element header.*

   The proposed SystemVerilog-2008 standard adds the ability to import package items into module, interface and program headers, making it easier to use package declarations as port and parameter types. *(Mantis 329)*

4. *Package chaining.*

   In SystemVerilog-2005, declarations imported into a package are not visible by way of subsequent imports of that package. The proposed SystemVerilog-2008 standard allows package imports to be chained, so that a package can specify that imported declarations are to be made visible in subsequent imports. *(Mantis 1323)*

5. *Automatic package declarations.*

   In SystemVerilog-2005, modules, interfaces, and programs can be declared with an **`automatic`** lifetime. This changes the default lifetime of all tasks and functions within the module, interface, or program to be automatic instead of static. The proposed SystemVerilog-2008 standard also allows packages to be declared with an **`automatic`** lifetime. *(Mantis 1524)*

6. *Localparam definitions in ANSI-style headers.*

   Verilog-2005 allows **`parameter`** constants to be declared as part of ANSI-style module declarations. The proposed SystemVerilog-2008 standard extends ANSI-style module declarations to also allow **`localparam`** constants. *(Mantis 1134)*

7. *Default input values for ports.*

   In Verilog-2005 an unconnected input port would resolve to the undriven value of its net type, typically high-impedance. This enhancement allows input ports to be defined with a default value which will be used when the port is left unconnected. One usage will be to allow adding new input ports to model without having to modify designs that currently instantiate the model without those new ports. *(Mantis 1619)*

8. *Bit selects and part selects of expressions.*

   In Verilog-2005, bit selects and part selects can only be applied to nets and variables. The proposed SystemVerilog-2008 standard allows bit selects and part selects of expressions. For example: `{a & b | c}[4:2]` will return bits 4 down to 2 of the expression result. *(Mantis 1197)*

9. *Task to invoke operating system commands.*

   The **`$system`** task allows SystemVerilog code to call operating system commands. Most Verilog simulators already have this task, but it was never part of the Verilog standard. *(Mantis 1863)*

10. *Alternate syntax for timeunit.*

    SystemVerilog-2005 added the ability to specify simu-

1. "Mantis" is the data base system used by the IEEE 1800 SystemVerilog standards committee to track bug reports and enhancement requests for Verilog and SystemVerilog. The Mantis item number has been included primarily for the convenience of the author in order to write and maintain this paper.

lation time units and time precision within a module using the keyword pair **timeunit** and **timeprecision**. The proposed SystemVerilog-2008 allows both the time units and time precision to be specified with just the **timeunit** keyword. *(Mantis 1623)*

11. *Synthesis parallel_case equivalent statement.*

    SystemVerilog-2005 has a **priority** construct, which defines that a **case** or **if** decision statement should be full (complete), and a **unique** construct, which defines that a decision statement should be both full and parallel (mutually exclusive). The proposed SystemVerilog-2008 standard adds a **unique0** construct, which specifies that a decision statement should be parallel, but does not need to be full. *(Mantis 2131)*

12. *Allow functions to spawn processes.*

    SystemVerilog-2005 does not allow functions to make nonblocking assignments. The proposed SystemVerilog-2008 standard removes this restriction.

    SystemVerilog-2005 also does not allow functions to spawn off execution threads, which can make some types of verification more difficult. The proposed SystemVerilog-2008 allows functions to spawn threads using **fork**...**join_none**. *(Mantis 1336)*

13. *Specifying severity levels with general print messages.*

    In SystemVerilog-2005, the **$fatal**, **$error**, **$warning**, and **$info** severity-level tasks can only be used in assertions. The proposed SystemVerilog-2008 standard will allow these severity-level tasks to be used anywhere $display can be used. *(Mantis 1641)*

14. *New print formatting specifiers.*

    SystemVerilog-2005 added aggregate data types such as unpacked structures, arrays, and unions, but it was only possible to print the individual members of these aggregates. The proposed SystemVerilog-2008 standard adds a **%p** format specifier which can be used to print all values contained in aggregate expressions.

    The proposed SystemVerilog-2008 standard also adds a C-like **%x** hexadecimal format specifier (equivalent to Verilog's **%h**). *(Mantis 331, 1749)*

15. *Specifying field widths in integer print formats.*

    Verilog-2005 does not allow specifying a specific field width when printing integer values. The proposed SystemVerilog-2008 standard extends the integer print formats to allow specifying field widths (e.g %5d). *(Mantis 1175)*

16. *Function to return a formatted string.*

    The proposed SystemVerilog-2008 standard adds a **$sformatf** system function which behaves like **$sformat**, except that the string result is passed back as the function return instead of as a task argument. *(Mantis 1589, 1651)*

17. *Add predefined macros for file and line number.*

    The proposed SystemVerilog-2008 adds C-like **`__FILE__** and **`__LINE__** macros, which allow access to the current file and line number from within SystemVerilog code. *(Mantis 1588)*

18. *SDF support for timing skew.*

    Verilog-2001 added the **$timeskew** and **$fullskew** timing skew checks. The proposed SystemVerilog-2008 standard defines how these checks are annotated from SDF files. *(Mantis 1140)*

19. *Default values for macro arguments.*

    Expands the capabilities of **`define** text substitution macros by allowing macros to be called without passing values to each macro argument. *(Mantis 1571)*

20. *Removing text substitution macros.*

    Verilog-2005 allows removing specific **`define** macro definitions using **`undef**. The proposed SystemVerilog-2008 adds **`undefineall**, which removes all previously defined macros. *(Mantis 1090)*

21. *Delete a queue.*

    In SystemVerilog-2005, only specific members of a queue can be deleted. The proposed SystemVerilog-2008 standard extends the queue **delete()** method to also allow deleting the entire queue. *(Mantis 1560)*

22. *Using external methods with parameterized class types.*

    SystemVerilog-2005 does not allow a class type to use both parameters and external methods. The proposed SystemVerilog-2008 standard makes this legal. *(Mantis 1857)*

23. *Action blocks in assume property statements.*

    The proposed SystemVerilog-2008 standard adds the ability to specify pass and fail action statements in **assume property** statements, making assume statements orthogonal to **assert property**. *(Mantis 1460)*

24. *Covergroup sample method with arguments.*

    The proposed SystemVerilog-2008 standard allows cover groups to be used with assertions without having to write special glue code. *(Mantis 2149)*

25. *Static variable in-line initialization*

    SystemVerilog-2005 allows local variables in tasks, functions and **begin**...end blocks to be initialized as part of the local variable declaration. This can lead to subtle coding errors because it is not obvious when a variable is static and therefore only initialized once before simulation starts running. the proposed SystemVerilog-2008 standard that the static local variables with in-line initialization be explicitly declared with the **static** keyword. *(Mantis 1556)*

26. *Local variable initialization in assertions.*

    SystemVerilog-2005 allows local variables to be declared in properties and sequences, but they cannot be directly initialized. The proposed SystemVerilog-2008 adds the ability to initialize these local variables at the time of declaration. *(Mantis 1668)*

27. *PSL-like assertion operators.*

    The proposed SystemVerilog-2008 standard adds 4 new operators that allow PSL-like shortcuts in assertions:

    - `##[+]` is equivalent to `##[1:$]`
    - `expr[+]` is equivalent to `expr[*1:$]`
    - `##[*]` is equivalent to `##[0:$]`
    - `expr[*]` is equivalent to `expr[*0:$]`

    (Mantis 1466)

28. *Logical implication and equivalence operators.*

    The proposed SystemVerilog-2008 standard adds a `->` logical implication operator and a `<->` logical equivalence operator.

    `expression1 -> expression2` is a shorthand for `(!expression1 || expression2)`.

    `expression1 <-> expression2` is a shorthand for `((expression1 -> expression2) && (expression2 -> expression1))`.

    (Mantis 1758)

29. *Overlapping multi-clock assertions.*

    In SystemVerilog-2005, the assertion operators `##0`, `|->` and `if...else` can only be used when the operands use the same clock. The proposed SystemVerilog-2008 relaxes this restriction to allow these operators to be used in multi-clock environments. *(Mantis 1683)*

30. *New value sample function.*

    The proposed SystemVerilog-2008 standard adds a `$changed` value sample function for use in assertions and other verification code to determine if an expression changed value during a clock cycle. *(Mantis 1677)*

31. *Assertions can use values sampled on a different clock.*

    In SystemVerilog-2005, sampled value functions, such as `$rose` and `$past`, must sample on the same clock as the assertion. The proposed SystemVerilog-2008 standard allows the sampled value functions to use a different clock than the assertion. *(Mantis 1731)*

32. *Assertion action control system tasks.*

    The proposed SystemVerilog-2008 standard adds new system tasks that give control over the execution of assertion pass and fail statements. The tasks are: `$assertpasson`, `$assertpassoff`, `$assertfailon`, `$assertfailoff`, `$assertnonvacuouson`, `$assertvacuousoff`. *(Mantis 1361)*

33. *Inferred assertion expression query functions.*

    The proposed SystemVerilog-2008 standard adds three system functions which can aid in creating generic assertion libraries: `$inferred_clock`, `$inferred_disable` and `$inferred_enable`. *(Mantis 1674)*

34. *Global clocking definition.*

    To aid in formal verification, the proposed SystemVerilog-2008 standard adds the ability to specify a global clocking definition for use in assertions. *(Mantis 1681)*

35. *Global clock past and future value sample functions.*

    The proposed SystemVerilog-2008 standard adds new assertion query functions that allow checking expression values one global clock cycle in the past or to evaluate expression values that will occur one global clock cycle in the future. These query functions are: `$past_gclk`, `$rose_gclk`, `$fell_gclk`, `$stable_gclk`, `$changed_gclk`, `$future_gclk`, `$rising_gclk`, `$falling_gclk`, `$steady_gclk`, `$changing_gclk`. *(Mantis 1682)*

Enhancements being considered

At the time this paper was presented (21 February 2008) the SystemVerilog standards committee was still considering several important enhancements. It is likely that these enhancements will be approved for inclusion in the proposed SystemVerilog-2008 standard.

36. *Assertion checkers.*

    The proposed SystemVerilog-2008 standard is considering adding an assertion library modeling construct, referred to a "checkers". This construct would replace the current use of modules to encapsulate assertions in libraries such as OVL. *(Mantis 1900)*

37. *New assertion building block statement.*

    The proposed SystemVerilog-2008 standard is considering adding a new `let` statement for defining reusable assertion building blocks. *(Mantis 1728)*

38. *Linear Temporal Logic (LTL) operators.*

    Allow for strong and weak operations for formal verification. The proposed new operators (subject to change) are: `#-#`, `#=#`, `next`, `s_next`, `until`, `s_until`, `until_with`, `s_until_with`, `implies`, `always`, `s_always`, `eventually`, `s_eventually`, `if...else`. *(Mantis 1932)*

39. *Asynchronous assertion aborts.*

    The proposed SystemVerilog-2008 standard is considering adding new `reject_on` and `accept_on` operators that can cause an active assertion thread to abort asynchronously as either a pass or a fail. *(Mantis 1757)*

40. *Deferred immediate assertions.*

    The proposed SystemVerilog-2008 standard is considering adding a way to defer execution of an immediate assertion within a simulation time step. This can help prevent race conditions between the assertion and the value being tested. *(Mantis 2005)*

41. *Elaboration error tasks.*

    The proposed SystemVerilog-2008 standard is considering adding the ability to check conditions during elaboration time, before simulation begins to run, and print out messages with severity levels, similar to assertion severity messages. A fatal severity level would cause elaboration to abort, without running simulation. *(Mantis 1769)*

42. *Concurrent assertions in loops.*

    The proposed SystemVerilog-2008 standard is considering allowing concurrent assertions to be executed from within **`for`** and **`foreach`** loops. Each pass of the loop starts a new assertion thread which uses the loop control values of that pass of the loop. *(Mantis 1995)*

43. *New restrict property statement.*

    The proposed SystemVerilog-2008 standard is considering adding a **`restrict property`** statement, which can be used to define limits in the formal state space. *(Mantis 1806)*

44. Immediate assume and cover statements

    The proposed SystemVerilog-2008 standard is considering adding the ability to specify a non-temporal **`assume`** statement and **`cover`** statement that execute without creating a temporal thread. The new statements would execute the same as an immediate **`assert`** statement. *(Mantis 1726)*

45. *VPI support for objects.*

    The proposed SystemVerilog-2008 standard is looking at how to add Programming Language Interface (PLI) support for dynamic Object-Oriented verification constructs as part of the VPI library. *(Mantis?)*

46. VPI support for new SystemVerilog features.

    The proposed SystemVerilog-2008 standard is finalizing VPI support for all new features being added as part of the proposed SystemVerilog-2008 standard. *(various Mantis numbers)*

V. Conclusions

Digital hardware design has undergone tremendous changes over the 25 year history of the Verilog Hardware Description Language. Verilog has evolved along with the needs of digital hardware design and verification engineers. The latest generation of Verilog has a new name, "SystemVerilog". The specification of a proposed SystemVerilog-2008 standard is nearing completion, with plans for IEEE balloting and ratification by the end of 2008 (this date might slip to early 2009).

VI. About the author

Mr. Stuart Sutherland is a design engineer and SystemVerilog expert. He holds a BS in Computer Science, with an emphasis in Electronic Engineering, and has worked on a variety of designs. Stuart has been working with Verilog since 1988, and has been involved with the Verilog and SystemVerilog standards efforts since their beginning, in 1993. He is an active member of the IEEE 1800 SystemVerilog standards committee, and is the technical editor of the SystemVerilog Reference Manual and the Accellera Verilog-AMS reference manual. He was also an editor of the IEEE 1364-1995, 2001 and 2005 Verilog standards and Accellera SystemVerilog 3.0, 3.1 and 3.1a standards. Stuart founded Sutherland HDL, Inc. in 1992. His company specializes in providing expert training on Verilog, SystemVerilog, and the Verilog PLI. Stuart is the author or co-author of several books and papers on Verilog and SystemVerilog. (copies of these papers are available at http://www.sutherland-hdl.com/papers).

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