The Verilog PLI is Dead (maybe) ... Long Live the SystemVerilog DPI!

by Stuart Sutherland, Sutherland HDL, Inc.

The Verilog PLI Is Dead (maybe)...
Long Live The SystemVerilog DPI!

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Objectives

- Introduce the SystemVerilog DPI
- Verilog PLI strengths and weaknesses
- Show how the SystemVerilog DPI works
- Compare and contrast PLI and DPI
- Decide if the PLI is finally dead

presented at the Synopsys Users Group Conference, March 2004
A Review of Verilog Tasks and Functions

- The DPI is a new form of Verilog tasks and functions
- A Verilog task
  - Executes as a subroutine
  - Can advance simulation time
  - Does not have return values
  - Called as a programming statement

module chip (...);
  task sync_reset;
  resetN <= 0;
  repeat (2) @(posedge clock);
  resetN <= 1;
endtask

function int rotate (int a, b);
  return ({a,a} >> b);
endfunction

always @(negedge master_reset)
  sync_reset; //call task
always @(a, b, opcode)
  case (opcode) //call function
    ROR: result = rotate(a,b);
  endcase
endmodule

Overview of the DPI

- The SystemVerilog Direct Programming Interface:
  - “Imports” C functions into Verilog
  - Provides a new way to define a Verilog task or function

module chip (...);
import "DPI" function real sin(real in); //sin function in C math lib
  always @(a, b, opcode)
    case (opcode) //call function
      SINE: result = sin(a);
    endcase
  endcase
endmodule

Verilog code thinks it is calling a native Verilog task or function

- Using the SystemVerilog DPI
  - Verilog code can directly call C functions
  - Verilog code can directly pass values to and from C functions

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Verilog PLI Details

- Need to know how PLI works in order to compare to DPI...
- The Verilog PLI is a *simulation interface*
  - Reads/modifies simulation data structures
  - Does not read Verilog source code
  - Does not work with synthesis compilers or other tools

The PLI is a protecting layer between user programs and simulation data structure
  - *Indirect access* through PLI libraries
    - C program cannot directly read or modify the simulation data
    - Protects the simulator from bad C programs
    - Protects C programs from bad Verilog code

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Overview of the Verilog PLI

- The PLI allows users to extend Verilog by creating “user-defined system tasks and system functions”
  - Must begin with a dollar sign ($)
  - Called the same as with Verilog tasks and functions

```verilog
always @(a, b, opcode)
case (opcode) //call function
  SINE: result = $sine(a); // call a PLI application
```

- A system task/function invokes a “calltf routine”
  - A user-defined C function associated with the task/function name
    - Can indirectly read system task/function argument values
    - Can indirectly return values back to simulation

- Defining system task/function names and calltf routines is:
  - Complex
  - Varies from one simulator to another

PLI Libraries

- TF library (introduced in 1985)
  - Provides access to system task/function arguments
  - Provides synchronization to simulation time and events

- ACC library (introduced in 1989)
  - Extends TF library to access to design structure
  - Created to enable ASIC delay and power calculation

- VPI library (introduced in 1995)
  - Superset of TF and ACC libraries
  - Adds access to behavioral and RTL models

- NOTE! The IEEE is considering deprecating (removing) the TF and ACC libraries from the 1364 standard
  - Only the VPI library supports the new Verilog-2001 features
  - Only the VPI library will support SystemVerilog enhancements

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The Power of the PLI

- Supports system task/function arguments of any type
  - Data types, instance names, scopes, null arguments, etc.
  - Allows a variable number of task/function arguments
- Safe conversion of Verilog values to/from C values
  - Automatically converts any Verilog type to any C type
- Can find any modeling object anywhere in the data structure
- Can synchronize to simulation time
  - After blocking assignments, after nonblocking assignments, after all events, at future simulation times, etc.
- Can synchronize to any type of simulation event
  - Start, stop (breakpoints), finish, save, restart, logic value changes, strength level changes, RTL statement execution, etc.
- Supports multiple instances of system tasks/functions

The Disadvantages of the Verilog PLI

- Writing PLI applications is difficult to do
  - Must learn weird PLI terminology
  - Must learn what’s in the PLI libraries
  - Must create checktf routines, calltf routines, etc.
- Linking PLI applications to simulators is hard
  - Multiple steps involved
    - Different for every simulator
  - Who does the linking...
    - The design engineer?
    - A CAE tool administrator?
  - Managing multiple PLI applications is difficult
- PLI code is seldom binary compatible
  - Must re-compile for every simulator
What’s Next

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The DPI Makes Calling C Easy!

- The Direct Programming Interface makes it very simple for Verilog code to call C functions

```verilog
module chip (...);

import "DPI" function real sin(real in); //sin function in C math lib
always @a, b, opcode
  case (opcode) //call function
    SINE: result = sin(a);
  endcase

Verilog code directly calls the C function
```

- Can directly call C functions from Verilog
  - Do not need to define complex PLI system tasks/functions
- Can directly pass values to and from C functions
  - Do not need the complex PLI libraries to read/write values

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A Closer Look at the SystemVerilog DPI

- The Direct Programming Interface originates from:
  - The Synopsys VCS DirectC interface
  - The Co-Design Cblend interface (now owned by Synopsys)
- The Accellera standards committee
  - Merged the features of each donation
  - Added more functionality
  - Ensured full compatibility with the IEEE 1364 Verilog standard
  - Added rules for binary compatibility between simulators

More on DPI Import Declarations

- Import declarations can be anywhere a function can be defined
  - Within a Verilog module
  - Within a SystemVerilog interface
  - Within a SystemVerilog package
  - Within a SystemVerilog “compilation unit”
- Import declarations must have a prototype of the arguments
  - Must exactly match the number of arguments in the C function
  - Must specify compatible data types (details on a later slide)
- The same C function can be imported in multiple locations
  - Each prototype must be exactly the same
  - A better method is to define one import in a package
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Imported Function Arguments

- C functions can be imported as a Verilog task or function
  
  ```
  import "DPI" function real sin(real in); // sin function in C math lib
  import "DPI" task file_write(input string data, output reg status);
  ```

- The C function arguments can be imported as input, output or inout (bidirectional)
  - Arguments are assumed to be inputs unless declared otherwise

Task/Function Argument Data Types

- The import declaration must specify SystemVerilog data types that are compatible with the actual C function data types

<table>
<thead>
<tr>
<th>SystemVerilog Data Type</th>
<th>C Data Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>byte</td>
<td>char</td>
</tr>
<tr>
<td>shortsint</td>
<td>short int</td>
</tr>
<tr>
<td>int</td>
<td>int (32-bit)</td>
</tr>
<tr>
<td>longint</td>
<td>long long</td>
</tr>
<tr>
<td>real</td>
<td>double</td>
</tr>
<tr>
<td>shortsreal</td>
<td>float</td>
</tr>
<tr>
<td>chandle</td>
<td>void*</td>
</tr>
<tr>
<td>string</td>
<td>char*</td>
</tr>
<tr>
<td>enum (using default int type)</td>
<td>int</td>
</tr>
<tr>
<td>bit (2-state type, any vector size)</td>
<td>abstract array of int types</td>
</tr>
<tr>
<td>logic (4-state type, any vector size)</td>
<td>abstract array of int types</td>
</tr>
<tr>
<td>packed array</td>
<td>abstract representation</td>
</tr>
<tr>
<td>unpacked array</td>
<td>abstract representation</td>
</tr>
</tbody>
</table>

SystemVerilog types that map directly to C types

SystemVerilog types that require extra coding in C

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Using More Complex Data Types

- Structures and unions
  - Can be passed to equivalent C structures and unions
  - Must use compatible types within the structure or union
- Arrays (unpacked)
  - Can be passed to equivalent C arrays
  - Must use compatible types within the structure or union
  - The array indexing might change (C must always starts with 0)
- Vectors of 2-state data types (packed arrays of bit type)
  - Must be converted to integer arrays in C
  - Requires lots of extra coding in C
- Verilog 4-state data types (packed arrays of reg, wire, etc.)
  - Uses the Verilog PLI aval/bval encoding
  - Requires lots of extra coding in C

Compatibility Warning!

- It is the user's responsibility to correctly declare compatible data types in an import statement
  - Improper declarations can lead to unpredictable run-time behavior
  - The DPI does not check for type compatibility
  - The DPI does not provide a way to check and adjust for the data types on the Verilog side (the PLI can do this)
DPI Function Return Values

• A C function return value must be compatible with the basic SystemVerilog data types

<table>
<thead>
<tr>
<th>Imported Return Type</th>
<th>C Function Return Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>byte</td>
<td>char</td>
</tr>
<tr>
<td>short int</td>
<td>short int</td>
</tr>
<tr>
<td>int</td>
<td>int (32-bit)</td>
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<tr>
<td>long int</td>
<td>long long</td>
</tr>
<tr>
<td>real</td>
<td>double</td>
</tr>
<tr>
<td>short real</td>
<td>float</td>
</tr>
<tr>
<td>chandle</td>
<td>void*</td>
</tr>
</tbody>
</table>

Warning!

– It is the user’s responsibility to correctly declare an import statement that matches the C function return value

• Incorrect import declarations can lead to unexpected behavior

Pure, Context and Generic C Functions

• A pure function result depends solely on the function inputs

```cpp
import "DPI" pure function real sin(real, in);
```

– Must have a return value; cannot have output or inout arguments
– Cannot call any other functions or use static or global variables
– Can be highly optimized for simulation performance **Advantage**!

• A context function is aware of the Verilog scope in which it is imported

```cpp
import "DPI" context task print(input int file_id, input bit [127:0] data);
```

– Can be a void function, and can have output and inout arguments
– Can call functions from C libraries (for file I/O, etc.)
– Can call many of the functions in the PLI libraries (more on this later)

• A generic function is one that is not declared as pure or context

– Can be a void function, and can have output and inout arguments
– Can call other C functions
– Cannot call most functions in the PLI libraries
Declaration Warning!

You must do this right!

- It is the user’s responsibility to correctly declare pure and context functions
  - The DPI does not check for proper declarations
  - Improper declarations can lead to unpredictable simulation behavior
  - Improper declarations can lead to software crashes

Exporting Verilog Tasks and Functions

- Verilog tasks and functions can be exported to C
  - Exporting allows C code to call Verilog code
  - C thinks it is calling a native C function
  - C functions can synchronize to Verilog time by calling a Verilog task with time controls

```verilog
module chip (...);
  task sync_reset(inout resetN);
  resetN <= 0;
  repeat (2) @(posedge clock);
  resetN <= 1;
  endtask
  export "DPI" sync_reset;
  ...
endmodule
```

```c
function void C_model()
{
  ...
  sync_reset(rst); // call Verilog task
  ...
}
```

- C calling Verilog tasks and functions is unique to the DPI!
  - There is no equivalent in the PLI
Using the DPI with SystemC

- The DPI can be used to interface SystemC models with Verilog models
  - Verilog code can directly call an imported C function that connects to the SystemC model
  - Values can be directly passed to and from the SystemC model
- Using the DPI to interface Verilog with SystemC
  - Eliminates the need for a complex PLI interface
  - Eliminates the need for proprietary, non-portable interfaces

What’s Next

- Introduce the SystemVerilog DPI
- Verilog PLI strengths and weaknesses
- Show how the SystemVerilog DPI works
  - Compare and contrast PLI and DPI
  - Decide if the PLI is finally dead

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A Detailed Comparison of DPI versus PLI

- The paper contains a table that compares the DPI to the PLI
  - Show the unique capabilities of each interface

<table>
<thead>
<tr>
<th>DPI Interface</th>
<th>TF Interface</th>
<th>ACC Interface</th>
<th>VPI Interface</th>
</tr>
</thead>
<tbody>
<tr>
<td>Directly call C functions from Verilog code</td>
<td>Indirectly call C functions from Verilog code by associating the C function with a user-defined system task or system function name</td>
<td>(no equivalent)</td>
<td>(no equivalent)</td>
</tr>
<tr>
<td>C function can call Verilog function or task</td>
<td>Synch to simulator’s event scheduler</td>
<td>Synch to simulator’s event scheduler</td>
<td></td>
</tr>
<tr>
<td>(no equivalent)</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

A summary of the table is on the next two pages...

Does the DPI Replace the PLI?

- Advantages of the SystemVerilog DPI
  - Easy to use!
    - If compatible data types are used on both sides
  - A direct interface between Verilog and C
    - Directly passes values to/from C using task/function arguments
  - Can be optimized for performance
    - If pure functions are used (limits what the function can do)
  - C can call Verilog tasks and functions

- Weaknesses of the DPI
  - Fixed number of arguments
  - User is responsible to pass compatible data types
  - Cannot access simulation data structure
  - Cannot synchronize to simulation events or event queue

Danger!
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Does the DPI Replace the PLI?

- Advantages of the Verilog PLI
  - Allows access to entire simulation data structure
    • Find any Verilog object, anywhere in the design
  - Can synchronize to simulation
    • Synch to time (before or after blocking assignments, ...)
    • Synch to value changes, breakpoints, finish, ...
  - Provides an indirect access between Verilog and C
    • Protects simulation data structure from user C code
    • Automatically converts values between Verilog and C types

- Disadvantages of the Verilog PLI
  - Difficult to learn — even simple things are hard
  - Not binary compatible — different for every simulator
  - Can slow down simulator performance (significantly)

Using the DPI to Simplify the PLI

- DPI capabilities can be extended by using the PLI libraries
  - A DPI context function can call many of the PLI library functions
    • Eliminates creating a system task/function name (e.g. $sine)
    • Eliminates the complex PLI binding mechanism

- NOTE: The DPI context is not the same as the PLI context
  - DPI context is the scope in which the import declaration occurs
    • Matches the behavior of native Verilog task and functions
  - PLI context is the scope in which a system task is called
  - Context functions cannot fully utilize the PLI libraries
    • Cannot use PLI checktf and misctf routines
    • Cannot access all objects in the simulation data structure

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What’s Next

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☑ Verilog PLI strengths and weaknesses
☑ Show how the SystemVerilog DPI works
☑ Compare and contrast PLI and DPI
☑ Decide if the PLI is finally dead

Conclusion

• The Verilog PLI and the SystemVerilog DPI are both needed
• Use the DPI to
  – Directly call C functions that do not need to access the simulation data structure
  – Directly call PLI applications that only need limited access to the simulation data structure
  – Interface to C and SystemC models
• Use the PLI to
  – Access any object anywhere in the simulation data structure
  – Synchronize to the simulation event queue
    • Blocking assignments, nonblocking assignments, etc.
  – Synchronize to simulation events
    • Simulation start, stop, finish, save, restart, reset, etc.
Is the PLI Dead?

• We cannot chant:
  “The Verilog PLI is dead...long live the SystemVerilog DPI”
  – The DPI is great, but...
  – The PLI has many capabilities not in the DPI

• The correct chant is:
  “The PLI TF/ACC libraries are dead...
   long live the PLI VPI and
   the SystemVerilog DPI, together!”
  – The DPI greatly simplifies many applications
  – The VPI replaces the old TF and ACC libraries

Questions?
Supplemental:
About the Author

- Involved with Verilog since 1988
- Considered a Verilog PLI expert
  - Wrote that 800 page book on the PLI
- Member of IEEE 1364 standards group since beginning
  - Co-chair of the Verilog PLI task force
  - Editor of the PLI sections of the standard
- Member of Accellera SystemVerilog standards group
  - Editor of the SystemVerilog standard
- Develops and presents expert-level Verilog, PLI and SystemVerilog training courses

Supplemental:
PLI Standards

- OVI (now Accellera) PLI 1.0 (1990)
  - Standardized the original TF and ACC libraries
- OVI PLI 2.0 (1993)
  - Intended to replace PLI 1.0
  - Not backward compatible, so never implemented in simulators
- IEEE 1364-1995
  - Standardized PLI 1.0 as TF and ACC libraries
  - Rewrite of PLI 2.0 to be backward compatible, called VPI library
  - Adds the Direct Programming Interface (DPI) to Verilog
- Accellera SystemVerilog 3.1a (projected for April 2004)
  - Extends VPI library to support all SystemVerilog constructs
- IEEE 1354-2005 (2006 ?) [projected date]
  - Will include SystemVerilog DPI along with many VPI extensions
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Supplemental:
SystemVerilog Features

- Assertions test program blocks
- Clocking domains process control
- Interaces
- Nested hierarchy
- Limited port connect
- Enhanced literals
- Time values and units
- Specialized procedures

SystemVerilog from C / C++
- Classes dynamic arrays
- Inheritance associative arrays
- Strings references
- Int globals break
- Short int enum continue
- Long int typedef return
- Byte structures do-while
- Short real unions ++ -= *= /=
- Void casting >> << >>> <<< <<<
- Alias const & &= |= ^= %=

SystemVerilog ANSI C style ports generate
- Standard file I/O $value$plusargs
- Localparam 'ifdef 'else 'line
- Constant functions @

SystemVerilog Verilog-2001
- Modules wire reg
- Parameters begin-end += *= /=
- Library tasks * (power operator)
- Always @ $finish
- Assign $display
- Wire
- Time
- Fork-join
- elbow
- Type
- Memory
- 2D

SystemVerilog Verilog-1995
- Assign $finish $open $close
- Include 'timescale
- Wire reg
- Integer real
- Disable
- Events
- Time
- Wait @
- Fork-join
- 2D

Supplemental:
Import Function Arguments

- C functions can be imported as a Verilog task or function

```verilog
import "DPI" function real sin(real in); //sin function in C math lib

import "DPI" task file_write(input string data, output reg status);
```

- The C function arguments can be imported as input, output or inout (bidirectional)
  - Inputs behave as if copied into the C function when it is called
  - The C function should not modify input arguments
  - Outputs behave as if copied into Verilog when the function returns
  - Inouts behave as if copied in at call, and copied out at return
  - Arguments are assumed to be inputs unless declared otherwise

The “copying” values in and out of C functions describes the behavior.
Software tools can implement this behavior in many ways (using pointers, etc.)

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