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The Verilog IEEE 1364

PLI Task Force Report

Design Automation Conference
June 23, 1999

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The PLI Task Force

- The PLI task force of the Verilog Standards Group is:
  - Correcting errata in the 1995 Verilog PLI standard
  - Clarifying ambiguities in the 1995 standard
  - Defining enhancements for the 1999 standard
- The task force members are:
  - Chairman: Drew Lynch, Surefire Verification
  - Co-Chairman: Stuart Sutherland, Sutherland HDL
  - Guru: Charles Dawson, Cadence Design Systems
  - Guru: David Roberts, Cadence Design Systems
  - Guru: Steve Meyer, Pragmatic C

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Task Force Meetings

- The PLI task force meets two or more times each month
  - Meeting dates are posted on the task force web site
- Most business is conducted via phone conference
- Recommendations from the task force are presented to the main 1364 Verilog Standards Group for approval

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ACC/TF versus VPI

- The ACC and TF routines are being maintained
  - Correcting errata
  - Improving the documentation
- The VPI routines are evolving
  - Correcting errata and clarifying documentation
  - Adding new PLI features
    - For additional PLI capabilities
    - For new features being added in the Verilog HDL
  - *Enhancements to Verilog will only be incorporated in the VPI routines*

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Summary Of PLI Task Force Activity

- 328 proposed changes reviewed
  - 212 changes approved and incorporated in draft 2 of the proposed 1364-1999 LRM
    - Draft 2 is available for review
  - 27 additional changes approved for draft 3
  - 61 changes rejected or deferred
  - 28 changes currently being investigated
- A detailed description of each action item is available on the PLI task force web site:

  www.sutherland.com/pli_task_force/pli-tf_top.htm