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HDL

*The Verilog IEEE 1364*

*PLI Task Force  
Report*

IVC Conference, March 18, 1998

# The PLI Task Force

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- The PLI task force of the Verilog Standards Group is:
  - Correcting errata in the 1995 Verilog PLI standard
  - Clarifying ambiguities in the 1995 standard
  - Defining enhancements for the 1998 standard
- The task force members are:
  - Chairman: **Drew Lynch**, Surefire Verification
  - Co-Chairman: **Stuart Sutherland**, Sutherland HDL
  - Guru: **Charles Dawson**, Cadence Design Systems
  - Guru: **David Roberts**, Cadence Design Systems
  - Guru: **Steve Meyer**, Pragmatic C

# Task Force Meetings

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- The PLI task force meets one or two times each month
  - Meeting dates are posted on the task force web site
- Most business is conducted via phone conference
  - PLI errata is reviewed
  - PLI enhancement requests are discussed
  - Recommendations for corrections and enhancements are written
- Recommendations from the task force are presented to the main 1364 Verilog Standards Group for vote and approval

# Errata and Enhancement Summary

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- Status of PLI task force activity
  - 226 items reviewed
    - 130 items approved for incorporation in standard
    - 46 items rejected or deferred
    - 50 items currently being investigated
- The summary and detailed description of each action item is available on the PLI task force web site

[www.sutherland.com/PLI\\_task\\_force.htm](http://www.sutherland.com/PLI_task_force.htm)

# ACC/TF Routines versus VPI Routines

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- The ACC and TF routines are being maintained
  - Correcting errata
  - Improving the documentation
- The VPI routines are evolving
  - Correcting errata and clarifying documentation
  - Adding new PLI features
    - For additional PLI capabilities
    - For new features being added in the Verilog HDL
  - *Enhancements to the PLI will only be incorporated in the VPI routines*