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The Verilog IEEE 1364

PLI Task Force Report

IVC Conference, April 2, 1997

The PLI Task Force

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- The PLI task force of the IEEE 1364 working group comprises:
 - Members of the 1364 standards working group
 - Other interested PLI users and tool developers

- The task force is:
 - Correcting errata in the 1995 Verilog PLI standard
 - Clarifying ambiguities in the 1995 standard
 - Defining enhancements for the proposed 1998 standard

Task Force Organization

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- The PLI task force conducts most business via e-mail
 - PLI errata is reviewed
 - PLI enhancement requests are discussed
 - Recommendations for corrections and enhancements are written
- Correcting errata takes priority over enhancements
- Final recommendations from the task force are presented to the main 1364 working group for vote and approval

Errata and Enhancements

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- Errata reports are received from:
 - Verilog users
 - Members of the PLI task force
 - Each member is reviewing specific sections of the PLI standard
 - A recommended correction is identified for all errata
- Enhancements are received from:
 - Verilog users
 - Other 1364 task force groups (behavioral, ASIC, etc.)
 - A recommendation is made if the enhancement is needed and can be efficiently implemented

ACC/TF Routines versus VPI Routines

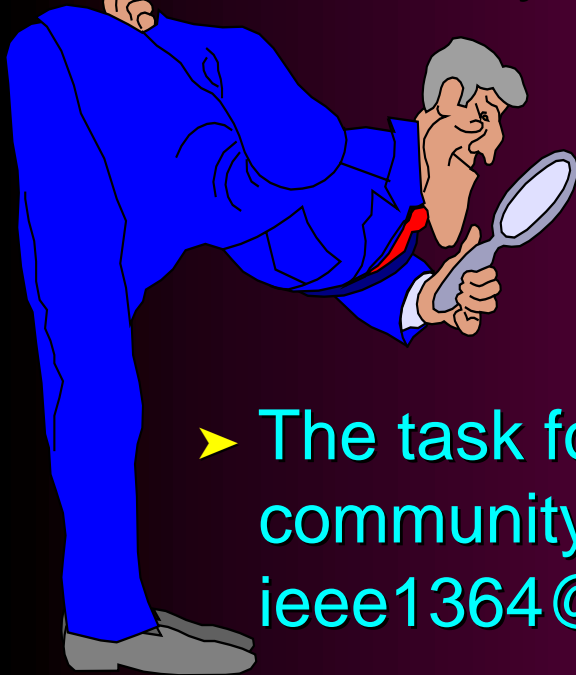
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- The ACC and TF routines are being maintained
 - Correcting errata
 - Improving the documentation
- The VPI routines are evolving
 - Correcting errata and clarifying documentation
 - Adding new PLI features
 - For additional PLI capabilities
 - For new features being added in the Verilog HDL
 - *New features in the PLI will only be incorporated in the VPI routines*

PLI Task Force Members

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- Most of the members of the PLI task force are EDA tool developers
 - More likely to find problems regarding implementation
 - Not as likely to find user-related problems



Your Input Is Needed!

- The task force strongly encourages the Verilog user community to send any and all PLI related issues to ieee1364@galaxy.nsc.com